Answers to exercises

Exercise 1.1

Decimal	1	2	4	8	16	32	64	128	256	512	1024
Hexadecimal	1	2	4	8	10	20	40	80	100	200	400
Binary	1	10	100	1000	1 0000	10 0000	100 0000	1000 0000	1 0000 0000	10 0000 0000	100 0000 0000

Exercise 1.2

15, 100

Exercise 1.3

100 0111,

11 1111 1111

Exercise 1.4

123, F00D

Exercise 1.5

291, 61453

Exercise 1.6

0010 0100 0110 1000

1010 1011 1100 1101

Exercise 1.7

F130 (hexadecimal)

Exercise 1.8

16, 32, 2^n

Exercise 1.9

FFFC = 1111 1111 1111 1100

Exercise 1.10

8, 9, 12

Exercise 2.1

A	B	C	A*(B+C)	A*B+A*C	A+(B*C)	(A+B)*(A+C)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	1
1	0	0	0	0	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

Exercise 2.2

(1) B

(2) Z*(X+Y)

(3) $\bar{X} * \bar{Y} = \overline{X + Y}$

(4) x*(Y+W)

(5) 0

(6) $\overline{X} * \bar{Y} + \bar{Z} = \overline{(X + Y) * Z}$

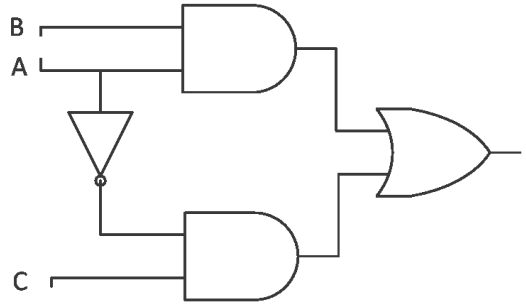
Exercise 2.3

$F = \bar{A} * \bar{B} * \bar{C} * D + \bar{A} * B * \bar{C} * D + A * \bar{B} * \bar{C} * D + A * \bar{B} * C * D + A * B * \bar{C} * D$

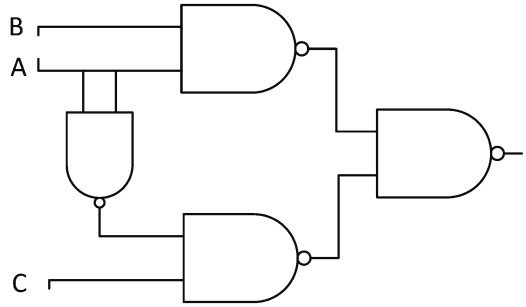
$+A * B * C * \overline{D} + A * B * C * D$

$= \bar{C} * D + A * D + A * B * C$

Exercise 3.1



Exercise 3.2



One 74HC00 chip

Exercise 3.3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR gate

Exercise 3.4

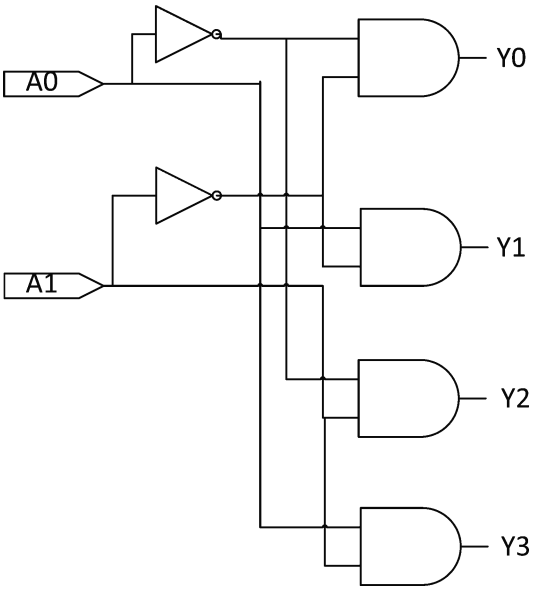
Two outputs are connected together. It will short circuit when the two outputs have different values.

Exercise 3.5

Two inputs tied together are not connected to any output. The value is unknown and likely to pick up noise.

Exercise 4.1

A1	A0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



Exercise 4.2

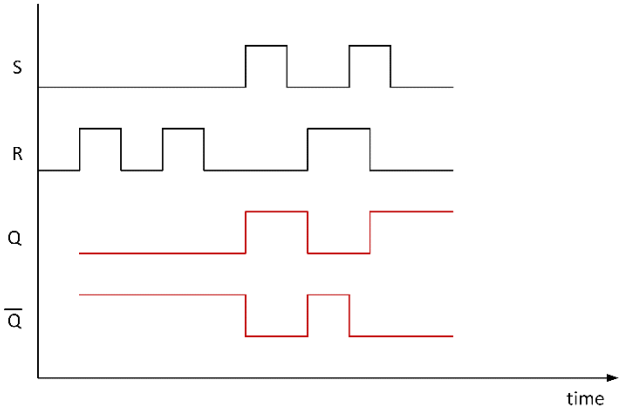
F = S0 XOR S1

Exercise 4.3

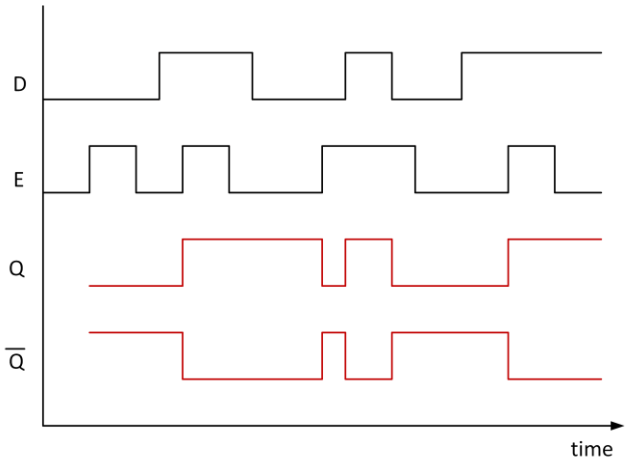
G = i0 XOR i1

H = i0 * i1 * i2

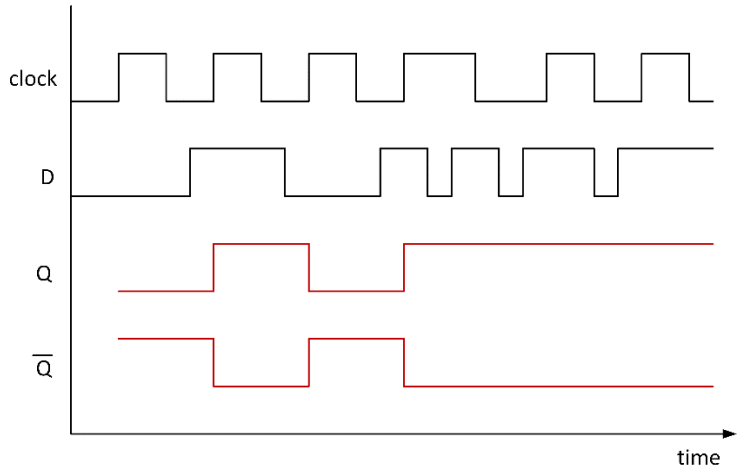
Exercise 5.1



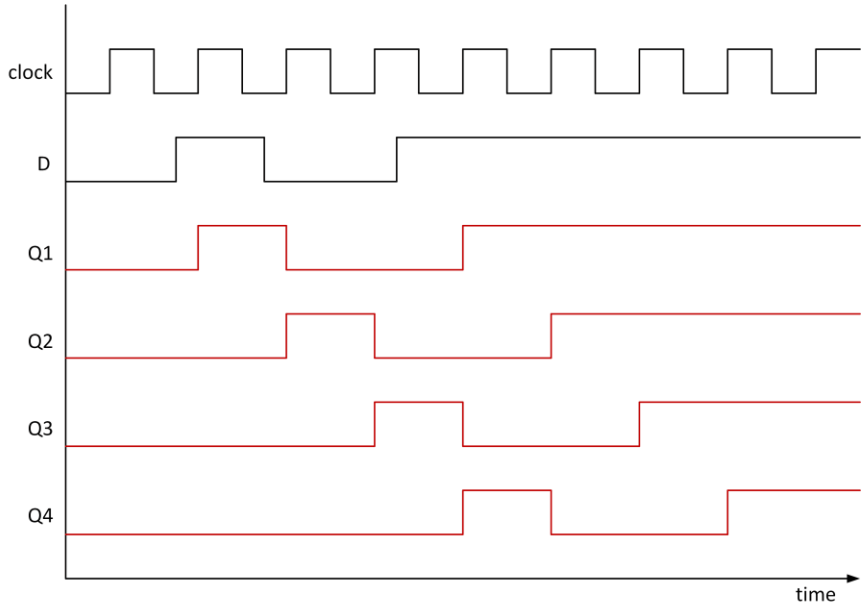
Exercise 5.2



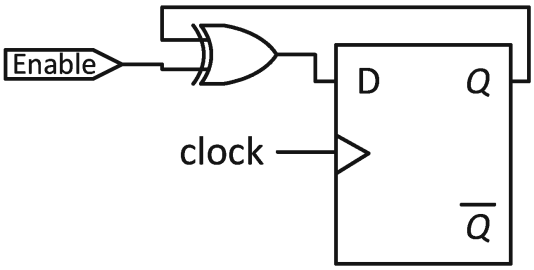
Exercise 5.3



Exercise 5.4



Exercise 5.5



Exercise 5.6

$Red = \overline{X1}$

$Yellow = X0$

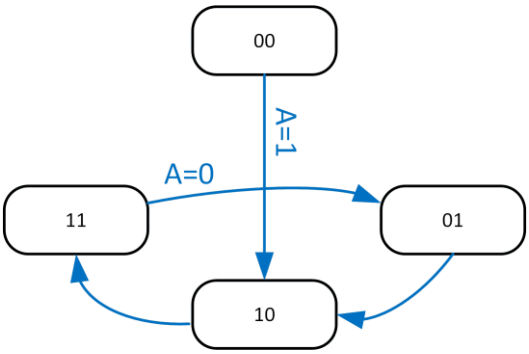
$Green = \overline{X0} * X1$

Exercise 6.1

inverter	combinational
decoder	combinational
multiplexer	combinational
D-latch	sequential
counter	sequential
adder	combinational
edge-triggered D flip-flop	sequential
shift register	sequential
state machine	sequential
next state logic	combinational
state memory	sequential
output logic	combinational

Exercise 6.2

A	Q1	Q2	Q1*	Q2*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1



Exercise 6.3

B	Q1	Q0	Q1*	Q0*
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

Q0* = Q1

Q1* = B XOR Q0